

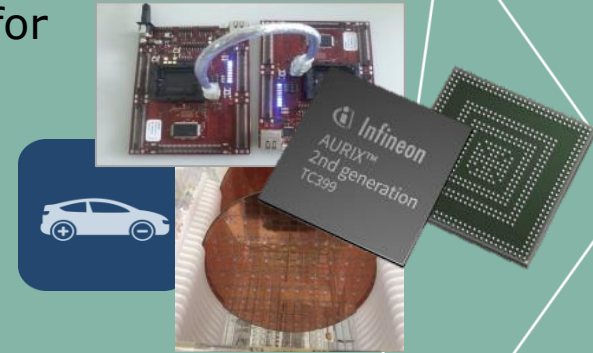
# Automotive High Performance Computing

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# Content

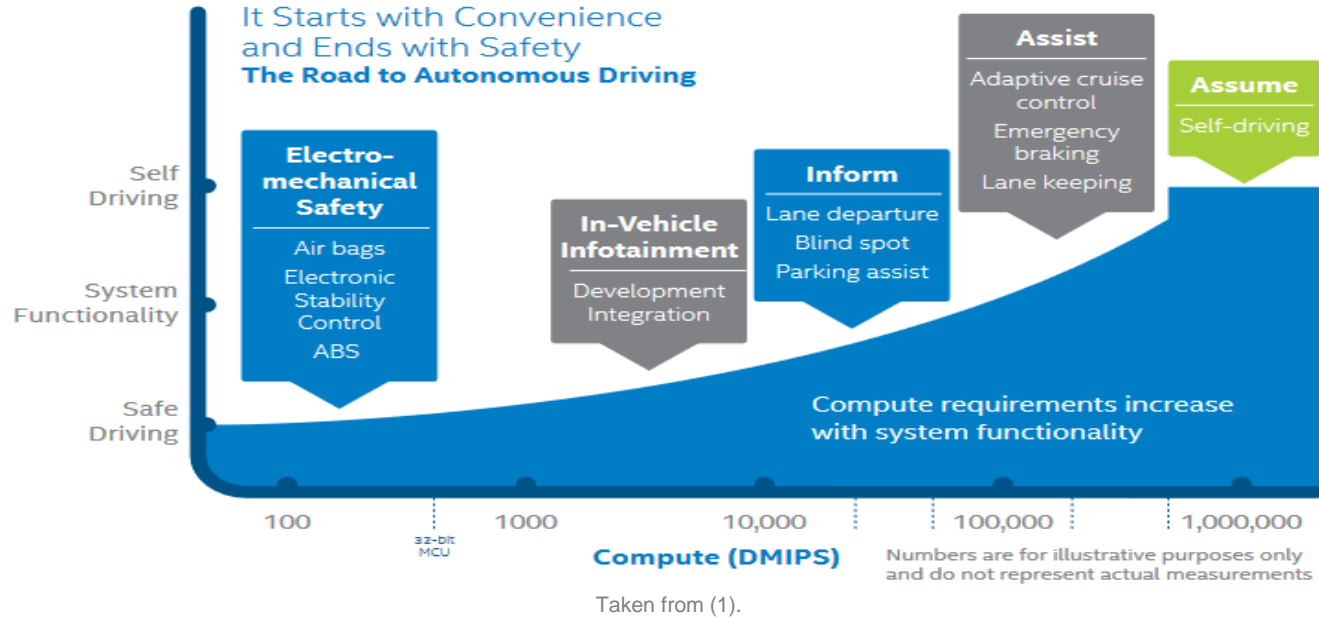
- 1 What will cars be like in the future?
- 2 Motivation - eHPC in Automotive
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- 4 Example - EPI European Processor Initiative
- 5 Closing remark

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# What will cars be like in the future?

## Autonomous cars demand more compute performance



(1) <https://www.intel.com/content/www/us/en/automotive/driving-safety-advanced-driver-assistance-systems-self-driving-technology-paper.html>

# What will cars be like in the future?

## Automotive systems are getting more and more complex

Accelerators for  
autonomous driving  
and big data

- Security
- AI (e.g. Fusion),  
Neuronal Networks

Scalable Safety  
Architecture  
Fail-safe → Fail-  
operational  
(ASIL B → ASIL D)

Enabling next  
generation of  
computing platforms  
2025 and beyond

High-integration of  
different in-vehicle  
domains (e.g chassis,  
body, AD, ..)

Special automotive  
requirements (e.g.  
extended temperatur  
ranges, ...) have to be  
considered.

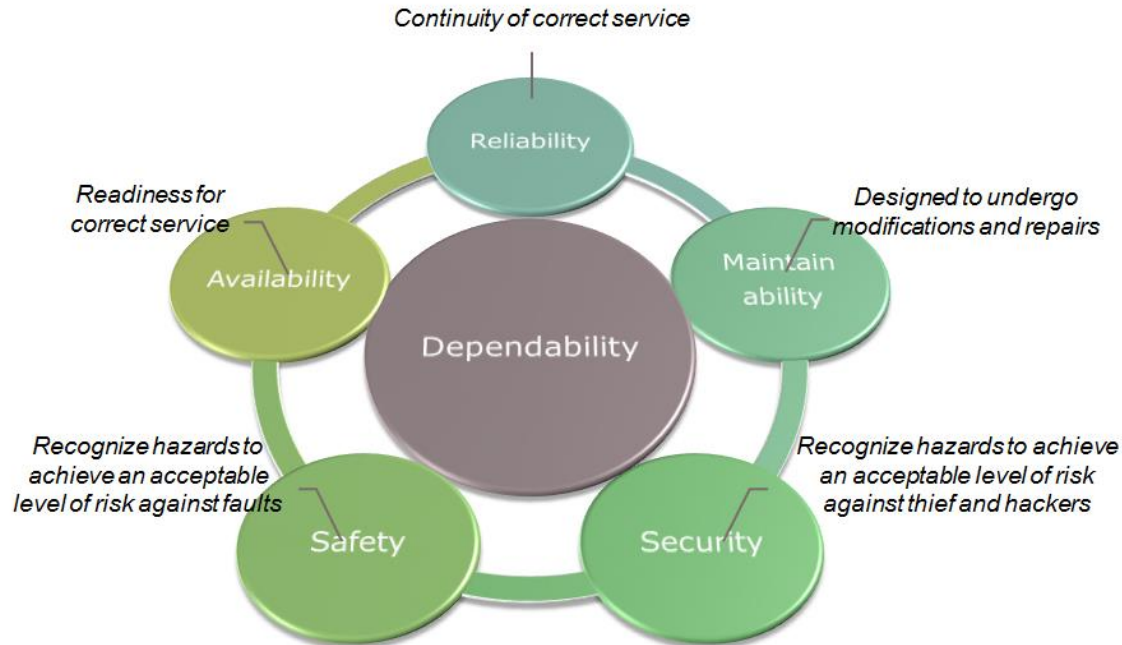
Hardware and  
software  
solutions

Processes,  
Methods and  
Tools

# What will cars be like in the future?

## Pursuing dependability

All requirements must be addressed as a whole





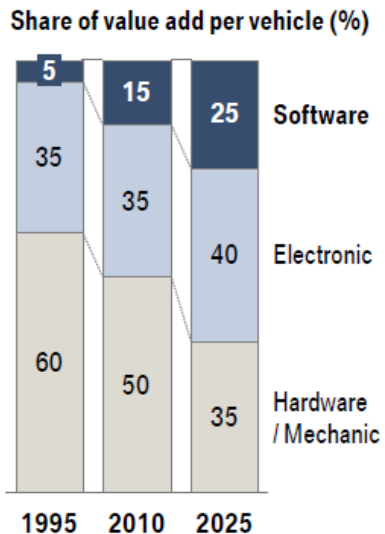
# What will cars be like in the future?

## Key applications relay on sufficient compute performance

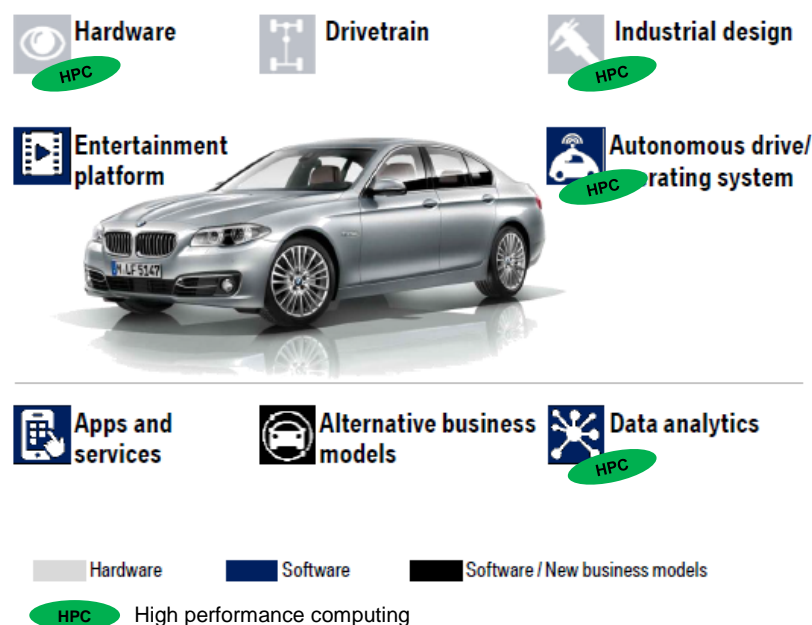
### KEY AUTOMOTIVE TRENDS FAVOUR SW-DRIVEN INNOVATION...

- A** AUTONOMOUS
- C** CONNECTED
- E** ELECTRIFIED
- S** SHARED

### ... LEADING TO INCREASED SHARE OF SW VALUE ADD ...



### ... AND CARS AS 'COMPUTERS ON WHEELS'



Source: AUTOMOTIVE SOFTWARE TECHNOLOGY – SHAPING TOMORROW'S ECOSYSTEM AUTOMOTIVESOFTWARE TECHNOLOGY – SHAPING TOMORROW'S ECOSYSTEM, C. Grote, 2017.

# What will cars be like in the future?

Degree of automation will directly depend on eHPC

## eHPC

*embedded High Performance Computing*

**Today**



**2030**



Increasing demand  
of computing power: **1000x**



## HPC

*High Performance Computing*

**Today**



**2030**

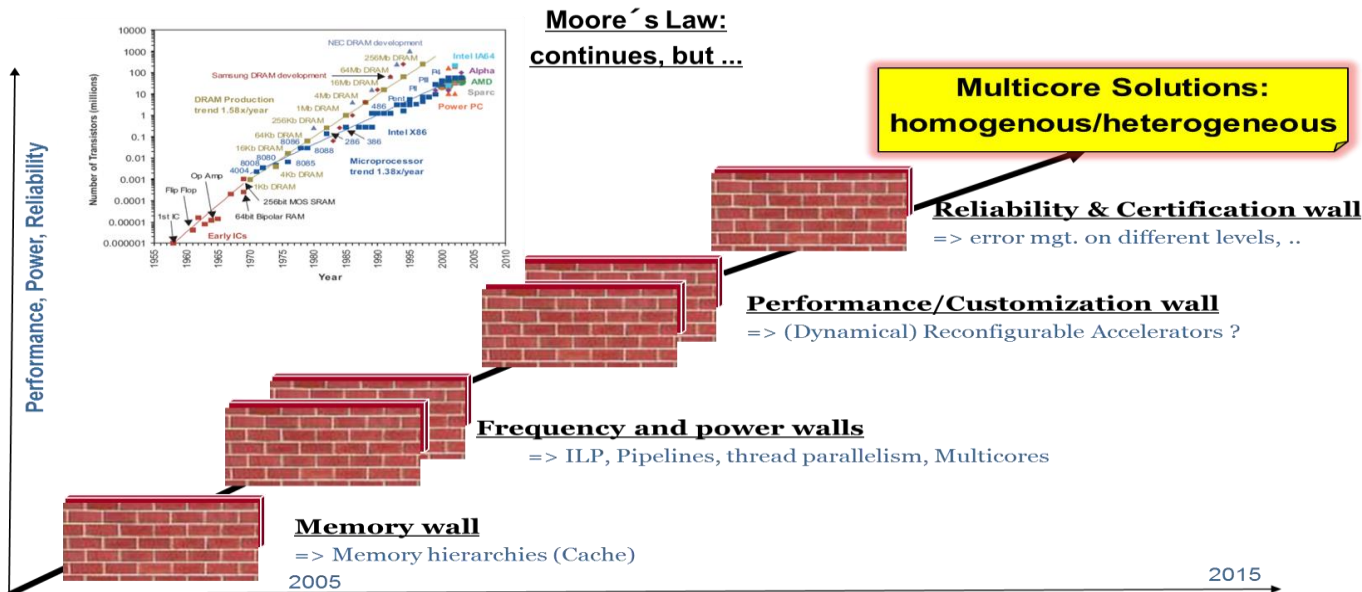


Increasing demand  
of computing power: **100 000x**



# What will cars be like in the future?

## Multi-Core is set on the Technology-Roadmap ...

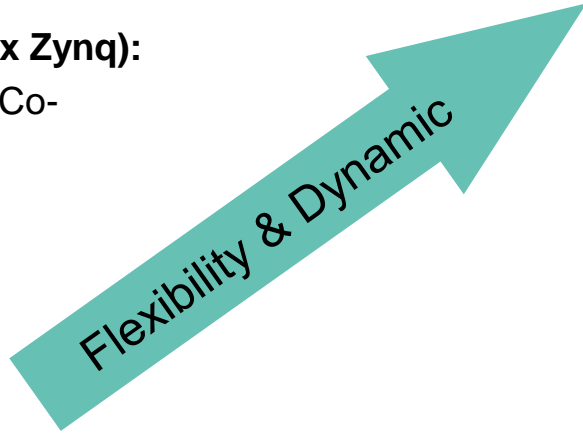
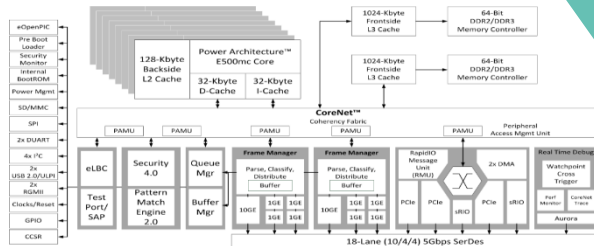


# What will cars be like in the future?

## Challenge flexibility and dynamic operation

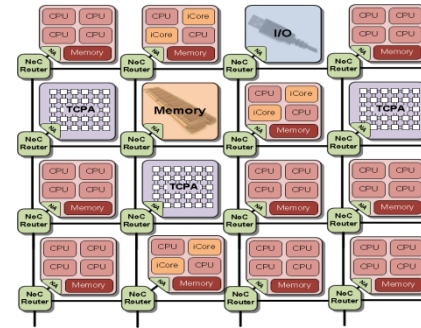
### Heterogeneous MPSoC (e.g. Xilinx Zynq):

- Integration of accelerators / Co-Processors
- Integrated COTS Multicore
- Increased customizability
- SW- und HW-Development (HW-SW Co-Design)



### Reconfigurable Architectures:

- Integration of accelerators / Co-Processors
- Fully customizable
- Dynamically reconfigurable
- Pure HW-Description



# What will cars be like in the future?

## Research Challenges of Embedded Multicores

- **Common resources shared between different execution units can lead to system dysfunction (malfunctions or loss of functions) caused by:**

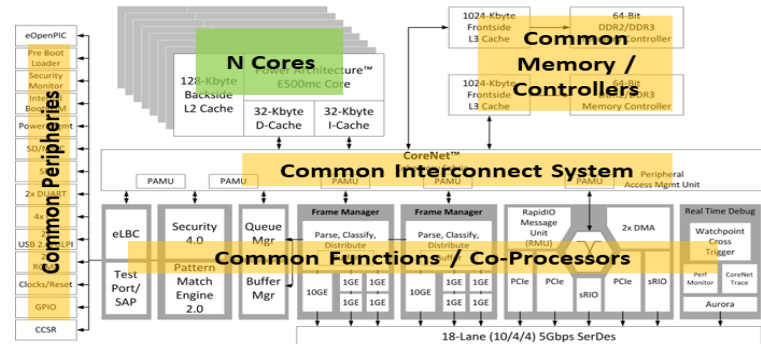
- Time interferences (determinism issues)
- Space interferences (segregation issues)
- Common Cause Failures (e.g. SEE)
- Race Condition

- **Issues depend on multicore architecture:**

- Mono-Bus / Multi-Bus / Crossbar / NoC / etc.
- Core local memory or only shared memory
- Lock-Step-Mode core / end2end ECC / etc.

- **Mitigations needed for safe and secure usage (per SW or HW):**

- Failure Detection: Monitoring, Voting
- Failure Isolation: Partitioning, Time Slicing / Deadlines, Budgeting
- Failure Correction: Function Recovery, Redundancy, Architectural Patterns

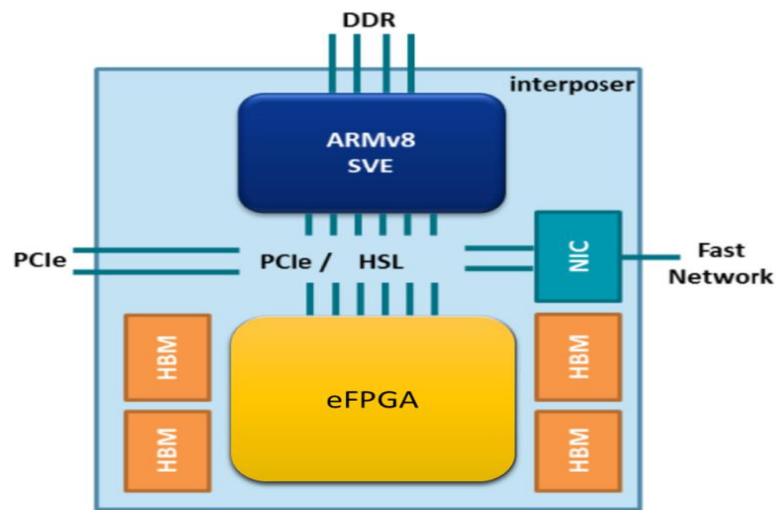


# What will cars be like in the future?

## Research topic: Embedded FPGA for Automotive



- Embedded FPGA for Safety, Security and Determinism
- Connection to „Monitoring Infrastructure“
- Configurable „Hardware Support“ for Determinism
  - Especially for Access to Peripherals
- Fail-Operational Hardware Support
  - By dynamic Reconfiguration
  - By dynamic Redundancy
  - Dynamic Migration
- Hardware Updates in Field



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# Motivation – eHPC in Automotive Innovation driver Autonomous Driving

## ■ Performance challenges in different domains

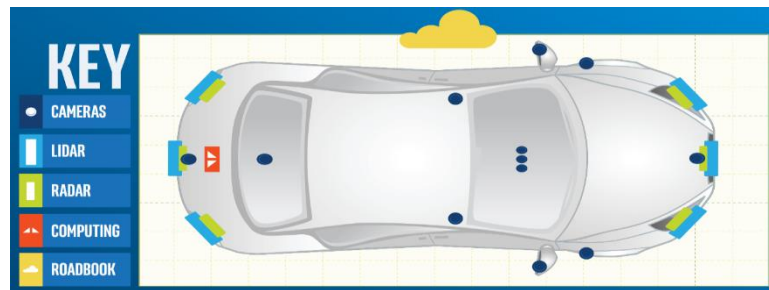
### ■ Computer vision

- Recognition (e.g. Intel i7)
- Image classification (Xilinx Everest)
- Semantic segmentation (NVIDIA PX2)

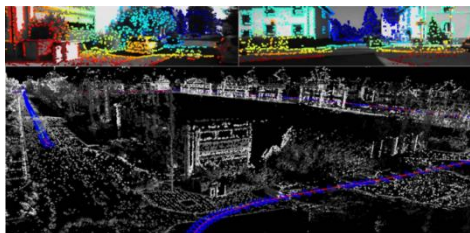
### ■ Data fusion

- Cameras
- Lidar
- Radar

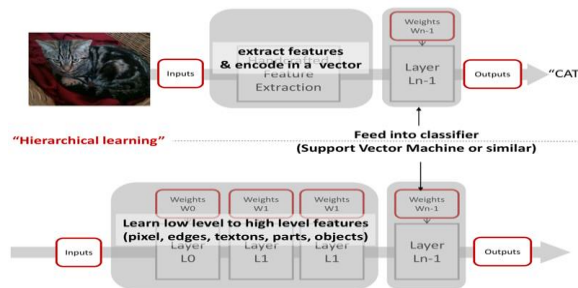
### ■ Connectivity / 5G (Intel Go)



Taken from (1).



Taken from (2).



Taken from (3).



Taken from (4).

(1) <https://newsroom.intel.de/news/sensors-the-eyes-and-ears-of-autonomous-vehicles/>

(2) <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=8237683>

(3) Xilinx, Inc. **Architectures for Accelerating Deep Neural Networks.**

(4) <https://blogs.nvidia.com/blog/2016/01/05/eyes-on-the-road-how-autonomous-cars-understand-what-theyre-seeing/>

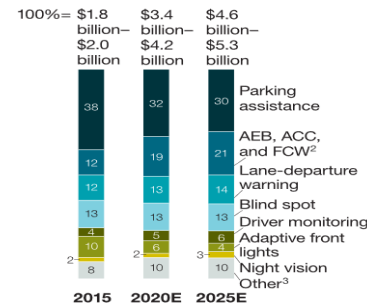
# Motivation – eHPC in Automotive Innovation driver Economic Importance



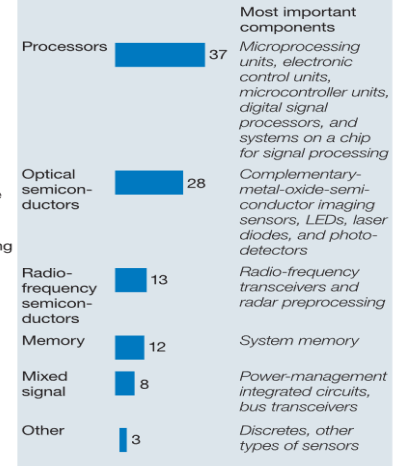
- Processors for ADAS will be a major source of revenue for semiconductor manufacturers
- Need to perform an increasing number of safety-critical and computation-intensive tasks
- State-of-the art solutions are unable to meet these requirements

For semiconductor companies, processors and optical semiconductors are expected to account for most hardware revenues for advanced driver-assistance systems in 2025.

**Semiconductor revenue in advanced driver-assistance systems per application, %<sup>1</sup>**



**Semiconductor revenue distribution on device types in 2025, %<sup>1</sup>**



<sup>1</sup>Figures may not sum to 100%, because of rounding.

<sup>2</sup>Autonomous emergency braking, adaptive cruise control, and forward-collision warning.

<sup>3</sup>Includes, among other categories, back-side monitoring and traffic-signal recognition.

McKinsey&Company

Taken from (1).

(1) <https://www.mckinsey.com/industries/semiconductors/our-insights/advanced-driver-assistance-systems-challenges-and-opportunities-ahead>



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# Snapshot - Current solutions for eHPC

## Intel - CPU combined with FPGA

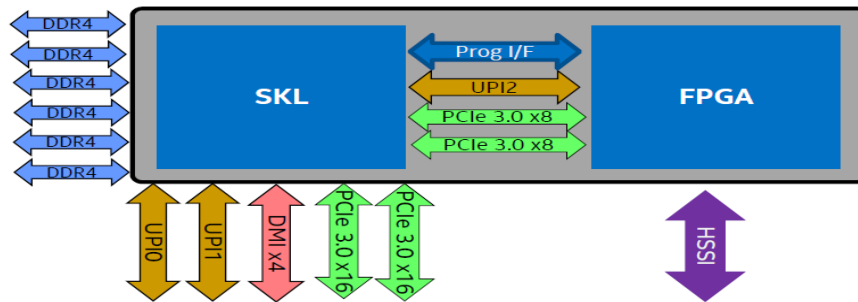
- Prototypes of autonomous cars usually built on top of conventional hardware
- High-end server CPUs combined with programmable FPGA logic

- e.g. Intel Xeon 6138P



Taken from (1).

## Skylake + FPGA on Purley



- Power for FPGA is drawn from socket & requires modified Purley platform specs
- Platform Modifications include Stackup, Clock, Power Delivery, Debug, Power up/down sequence, Misc IO pins (see BOM cost section)

Taken from (2).

(1) Jennifer Huffstetler. **Intel Processors and FPGAs—Better Together**. 2018.

(2) Ian Cutress. **Intel Shows Xeon Scalable Gold 6138P with Integrated FPGA, Shipping to Vendors**. 2018.

## ■ Lightweight ARM+FPGA solutions

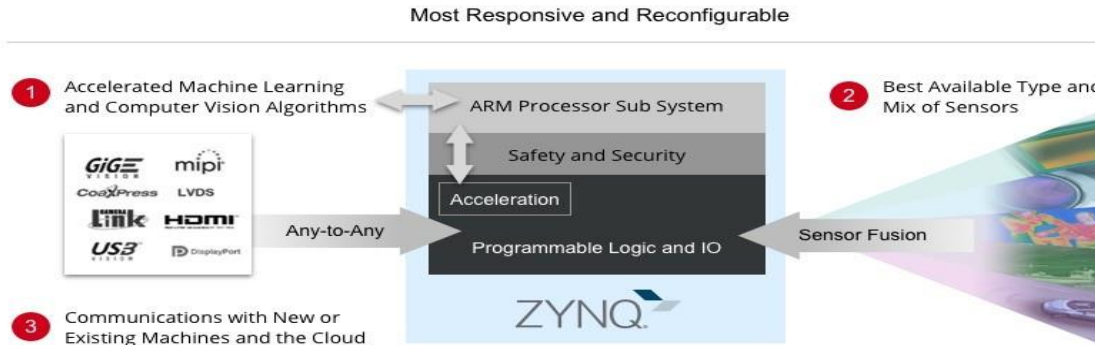
- General purpose CPU for non-critical software
- Complex operations mapped to FPGA (includes Machine Learning, Vision)
- Functional safety assured
- Low power design feasible

## ■ Available products include

- Xilinx Zynq, UltraScale MPSoC
- Intel Cyclone

## ■ Insufficient CPU performance for HPC

- e.g. Zynq-7000: Cortex-A9

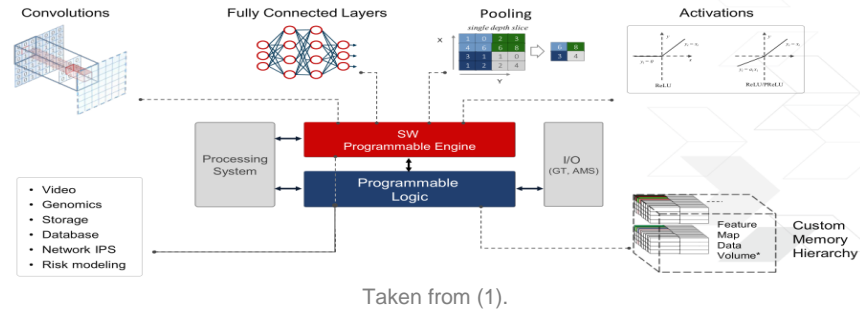
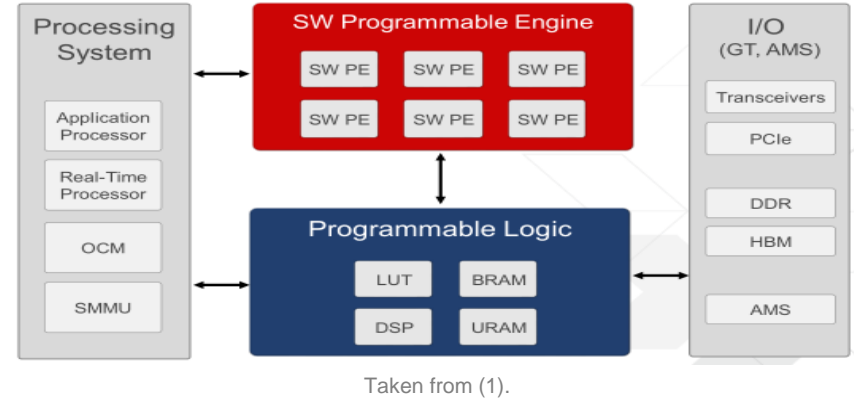


Taken from (1).

(1) <https://www.xilinx.com/products/design-tools/embedded-vision-zone.html>

## Xilinx Everest

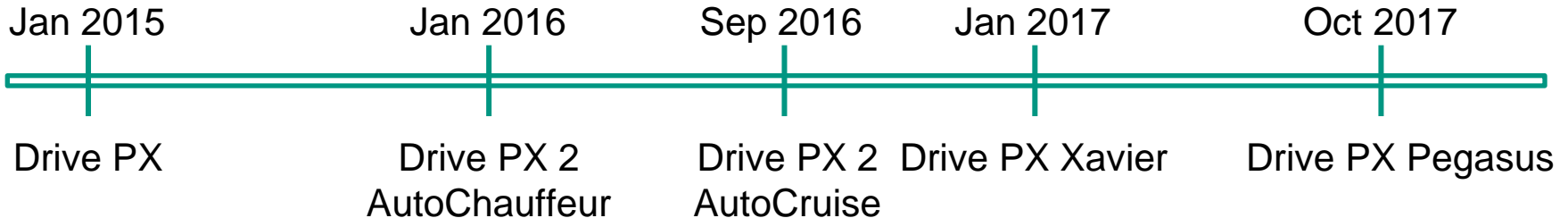
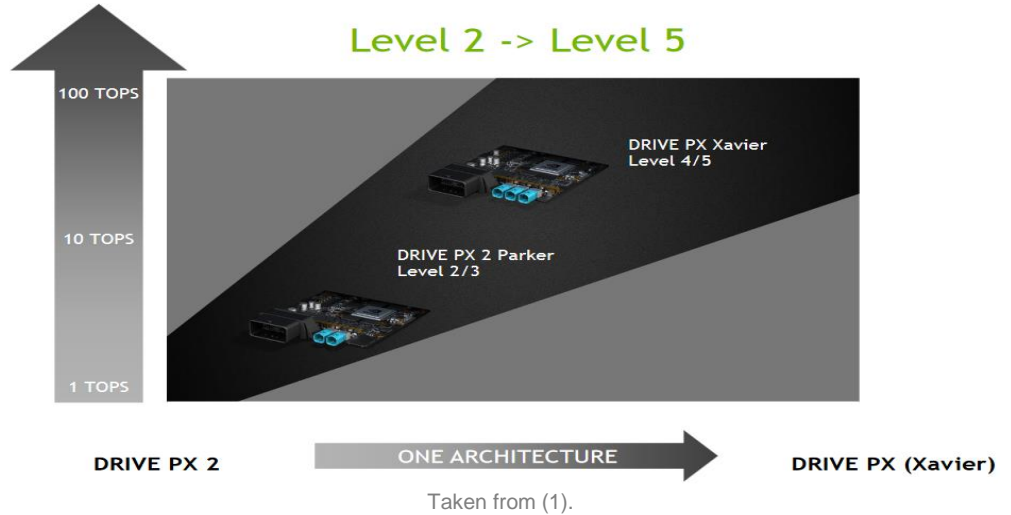
- Heterogenous architecture
  - Compute efficiency
  - Reduced power
  - Software programmable
  
- SW programmable engine
  - Domain specific architecture
  - Hardened 7nm technology
  - Throughput-oriented, low-latency
  
- Programmable logic
  - 'Soft' logic
  - Flexibility
  - Custom memory hierarchy



(1) Juanjo Noguera et al. **HW/SW Programmable Engine: Domain Specific Architecture for Project Everest**. Xilinx, Inx. 2018.

## ■ NVIDIA Drive PX series

- Computer boards for deep learning and autonomous driving
- Based on Maxwell, Pascal, and Volta GPU Microarchitecture
- Up to ASIL D



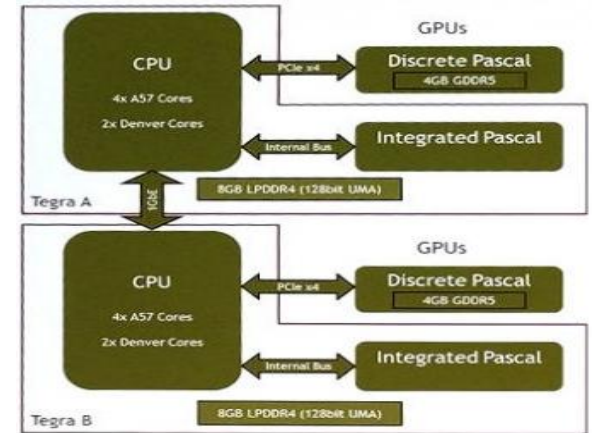
(1) Pradeep Kumar Gupta. **An overview of NVIDIA's autonomous vehicles platform.** NVIDIA. 2017.

## ■ NVIDIA Drive PX 2 AutoChauffeur (2016)

- 2x Tegra SoC, featuring each
  - 4x Cortex-A57
  - 2x Denver core
  - Pascal iGPU
  - 8GB LPDDR4 (50+ GB/s from CPU/iGPU)
- 2x Pascal discrete GPUs
  - 4GB GDDR5 (80+ GB/s from GPU)
- AURIX safety microprocessor
- Performance & Power
  - 24 DL TOPS, 8 TFLOPS
  - 250W TDP (board)
- e.g. used by Tesla for autonomous driving



Taken from (1).

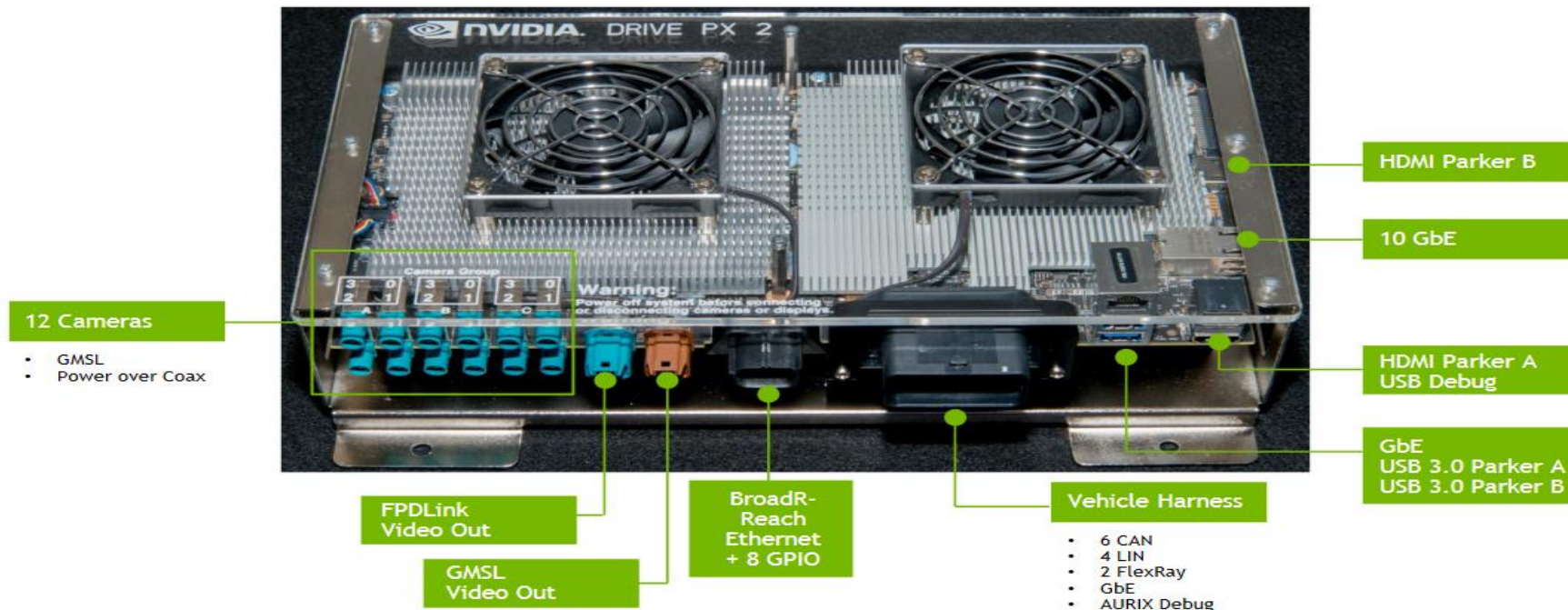


Taken from (1).

DRIVE PX 2

(1) <https://videocardz.com/58800/nvidia-drive-px-2-has-pascal-gpu-with-4gb-gddr5-memory>

## ■ NVIDIA Drive PX 2



Taken from (1).

(1) Pradeep Kumar Gupta. **An overview of NVIDIA's autonomous vehicles platform.** NVIDIA. 2017.



- NVIDIA Drive PX Pegasus
  - 2x Tegra Xavier SoC
    - 8-core NVIDIA custom Carmel ARM64
    - 1x Volta iGPU (512 CUDA cores)
  - 2x next-gen dGPU
  - AURIX TC3xx Safety Processor
  
- 16 GB LPDDR4
  
- Designed for ASIL D
  
- Performance & Power
  - 320 TOPS
  - 500W TDP (Board)

### ■ Advanced Driver Assistance System Platform

- Presented at CES 2014
- 2017: in Audi A8 series
- Used to enable level 3 autonomous driving

### ■ Contains

- NVIDIA Tegra K1 (later to be replaced by Tegra X1)
  - Quad-core Cortex-A15 with additional NVIDIA low-power processing unit
  - Kepler GPU (192 CUDA cores)
- Infineon Aurix
- Altera Cyclone FPGA
- MobilEye EyeQ3



Taken from (1).

# Snapshot - Current solutions for eHPC

## Comparison of Selected Devices



Device	TOPS	ASIL	DMIPS	TFLOPS	Remarks
NVIDIA Drive PX Xavier	30	C	–	6.3	A complete SoC with a GPU, CPU and accelerators.
NVIDIA Drive PX Pegasus	320	C / D	–	N/A	A computing platform. Contains an AURIX TC3xx safety processor.
AURIX TC39x	–	D	600	–	Fully compliant to ISO 26262.
Intel Go	100	C / D	–	1.5	Supports dedicated accelerator cards (e.g. FPGA).
Intel Xeon Platinum	5.2	QM	5000	3.6	Not designed for safety applications.
KALRAY MPPA	8	B	–	5	Up to 1024 cores.

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# Example - EPI European Processor Initiative

## Positioning the Project



EC Horizon2020



European 10 years research programme

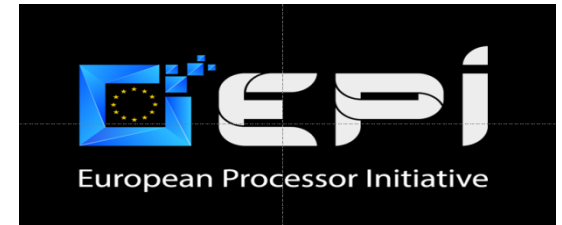


EU FPA call (ICT-42)



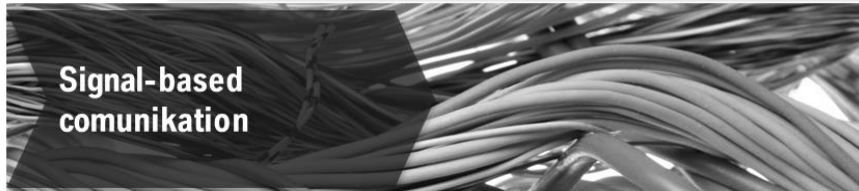
EPI European Processor Initiative

- European Approach for HPC-Technology for Exascale Super Computer
- HPC General Purpose Processor (GPP) by Bull/CEA
- Total: 120 M€ , 23partners, 4years, start: Oct 18
- eHPC GPP for Automotive, total 20M€ → AD
- Automotive core group:



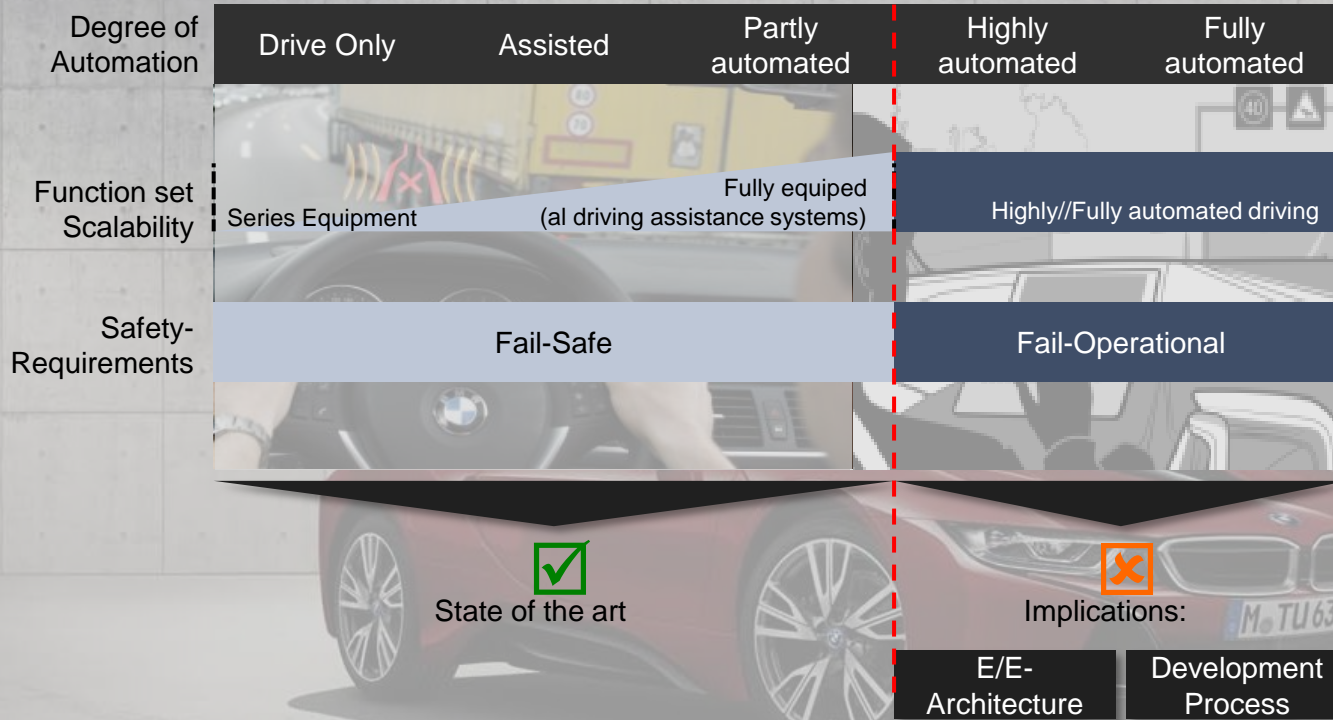
# Example - EPI European Processor Initiative

## Enabler next digitalization step in automotive E/E-Architecture



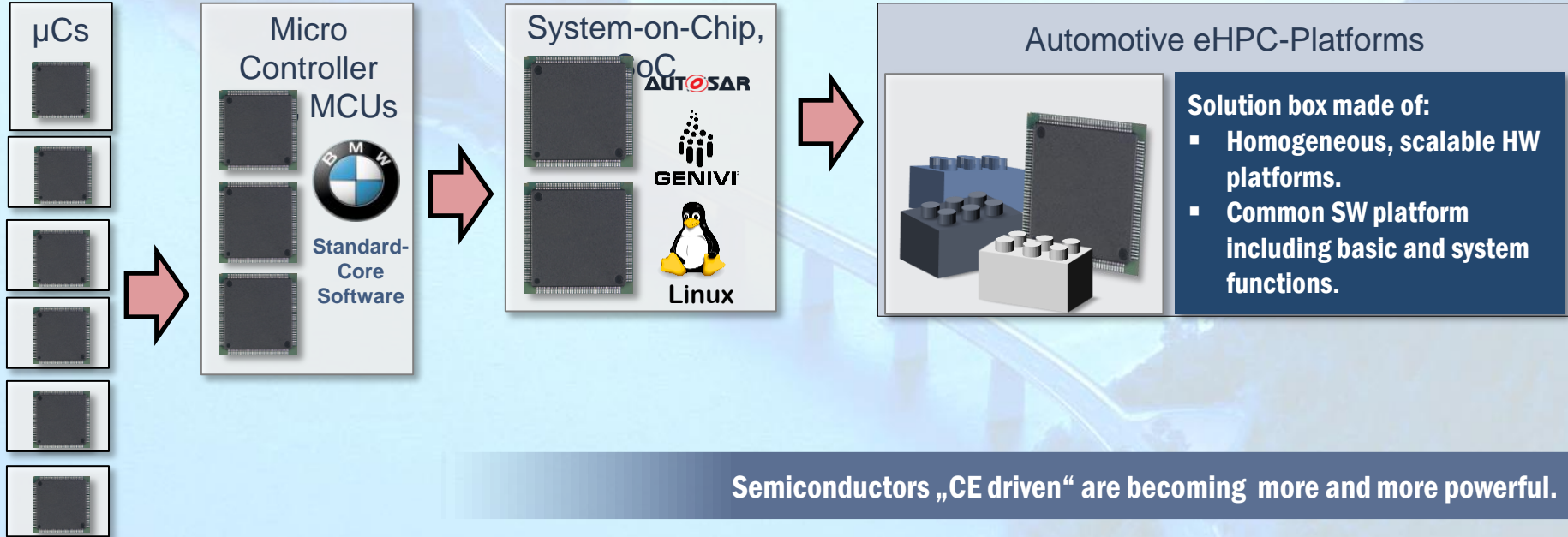
# Example - EPI European Processor Initiative

## Challenges for E/E-Architecture and development process





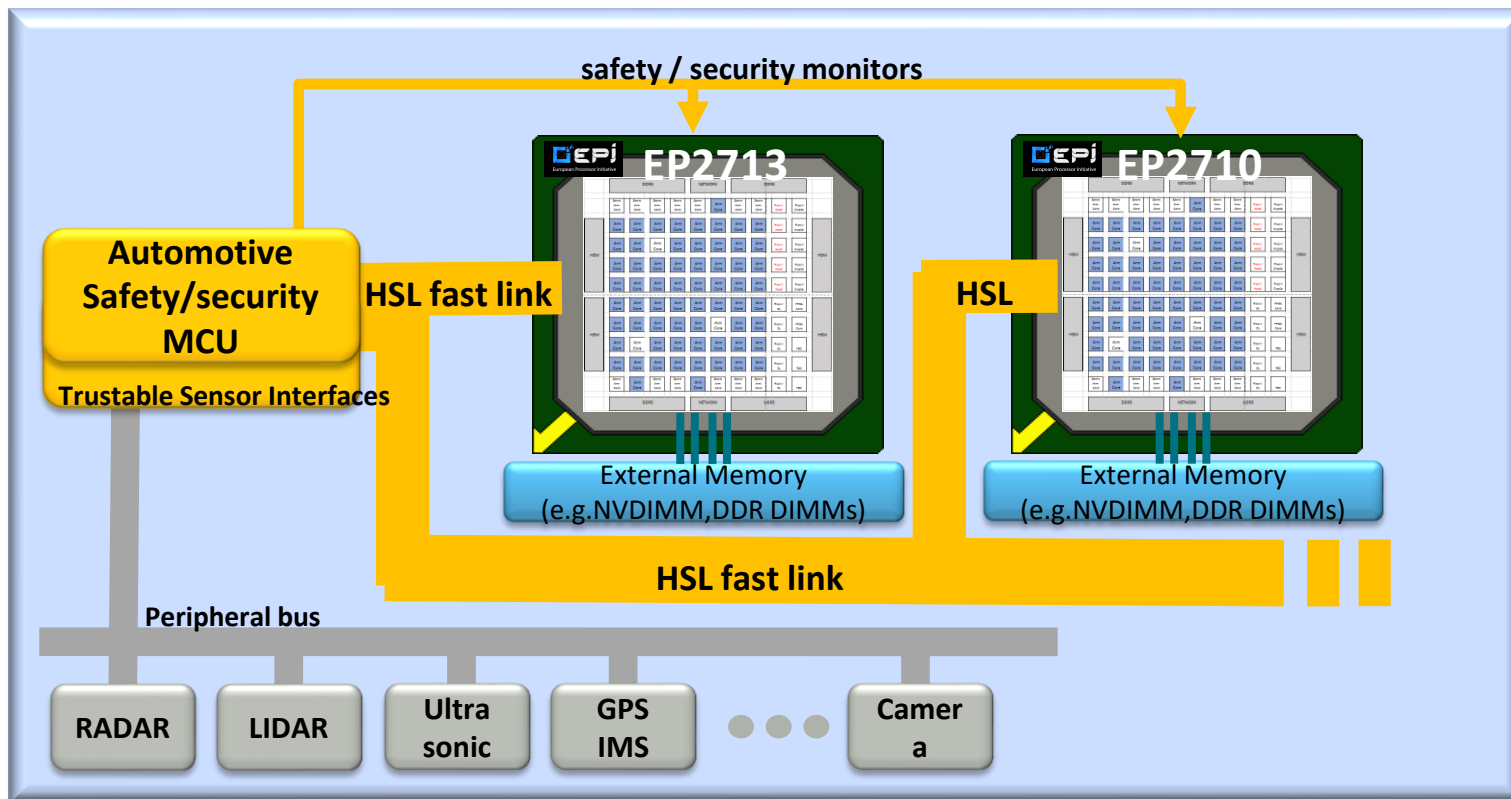
# Example - EPI European Processor Initiative CE-World CPUs enable highly performant compute platforms



Semiconductors „CE driven“ are becoming more and more powerful.

Across all industries the capability becomes apparent especially for performant processors.

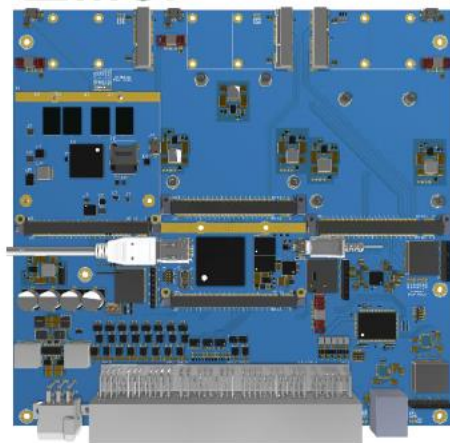
Powerful operating systems are increasingly used in automotive electronic control units.



\* eHPC – embedded HighPerformanceComputing

# Example - EPI European Processor Initiative

## EPI Demonstrator based on MODULAR COMPUTING PLATFORM



EPI-Demonstrator



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AD - still many aspects remain unclear and unsolved

Even if we will not drive totally autonomously, completely connected and fully electric by 2030 - does it mean that we have failed?

No! - any step taking us closer to ambitious vision should be recognized as a success!

... Active safety ... ADAS ... Highly automated driving in defined environments ...

.. and it is one thing to draw a big visionary picture, but it is another to accomplish the necessary details.

First of all, technology is not an end in itself!

..we do have to develop mature solutions and use cases that are ready for everyday use.

Research area: Artificial Intelligence; the topic is challenging enough.

Gives opportunity for industry to benefit from academia and institutes that are specialized in the field.

# Responsibility and commitment should be taken

Solutions for established infrastructures in Germany, France or Sweden? The established countries only represent a few percent of mankind.

Already today, European car makers act globally;  
and their cars run in the streets of Sao Paolo, Cairo or Bombay.

Emerging markets will become more and more important.  
New technologies must be flexible and meet different standards and infrastructures.

Apart from that:  
Never forget.. it takes 100% effort to achieve 90% of automation.  
..to scale it up to full automation, it takes another 100% on top.  
The last mile is always the hardest part of the run.





**Thank you very much for your  
kind attention!**

Part of your life. Part of tomorrow.

