Design and Fabrication of a SiC-Based Power Module with Double Sided Cooling for Automotive Applications

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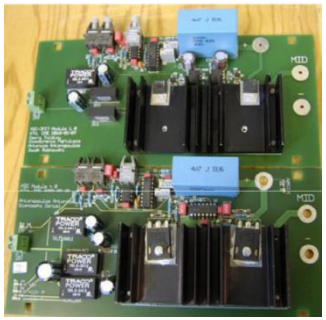
Contents

- Introduction
- Packaging Process of Power Modules with Double Sided Cooling
  - Substrate Preparation
  - Sintered Silver Materials
- Simulations
  - Thermal
  - Thermo-Mechanical
- Summary

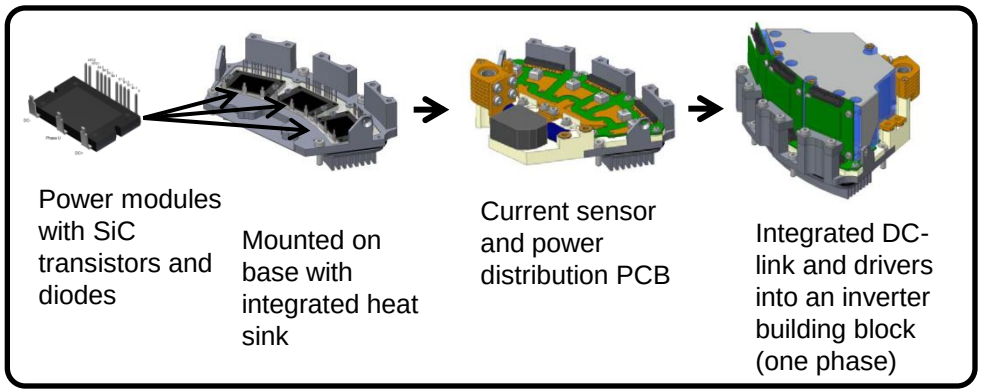
Device Packaging

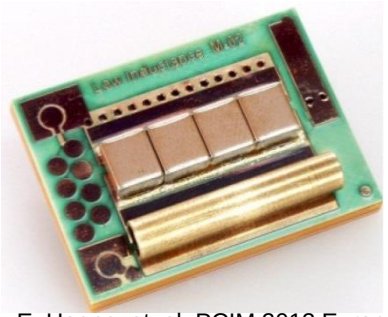
Three approaches to power device packaging:

- Discrete
  - Devices are all discretely packaged and connected with busbars or on PCB/DBC substrates.
- Modular
  - Power switching devices (transistors and diodes) are packaged in modules. A modular approach can be scaled to suit a range of application specifications and can be more compact.
- Embedded
  - Power device chips are embedded along with passives and driver electronics. Very compact and enables fast switching due to low inductance.



H-.P. Nee, ISiCPEAW, May 29-30, 2012, Stockholm, Sweden





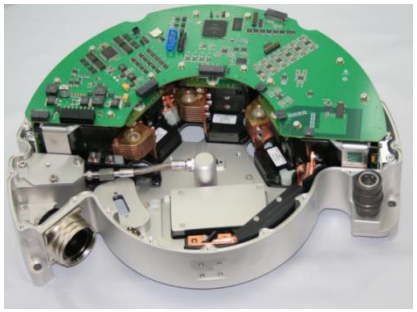
E. Hoene, et. al.,PCIM 2013 Europe Conference Proceedings, 198-205.

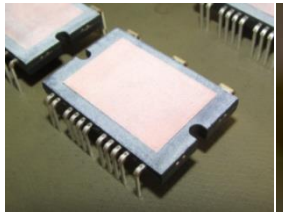
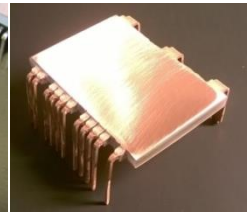
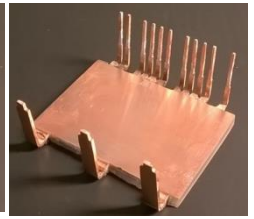
The COSIVU Project

- FP7 COSIVU project (Compact, smart and reliable drive unit for commercial electric vehicles)
- ***Power inverter needs to be highly integrated and compact.***
- ***SiC based power devices*** → Improved current density and thermal conductivity → smaller required chip area.
- ***Double sided cooling*** → lower thermal resistance → increased current carrying capability/chip area → smaller modules
- To maximize thermal performance sintered silver is used to connect the devices.







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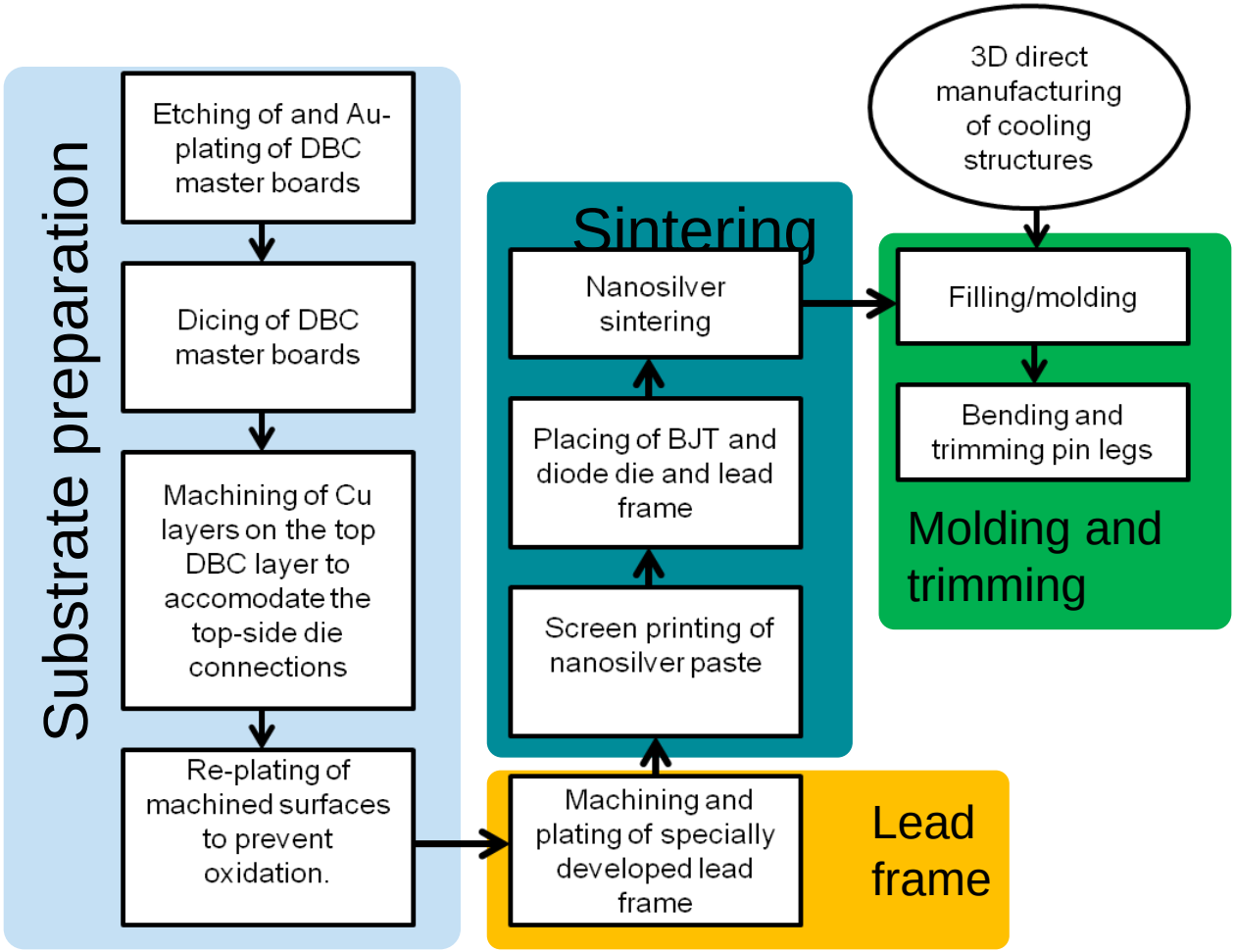
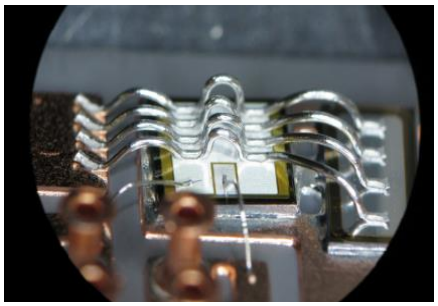
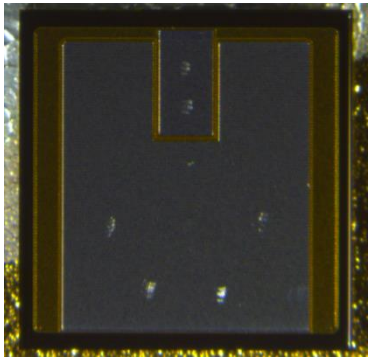
Packaging Process

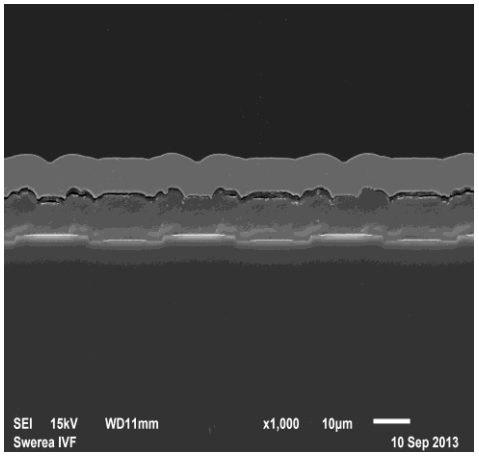


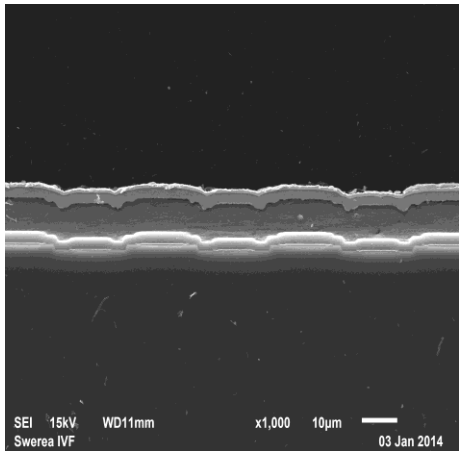
Substrate Preparation

- Problems:
  - Al top metallization
  - Non-conducting frame
- Initial plan: Electroless plating process
  - 20 µm Ni
  - 50-100 nm Au
- This would prepare surface for sintering process and create stand-off distance to the edge.



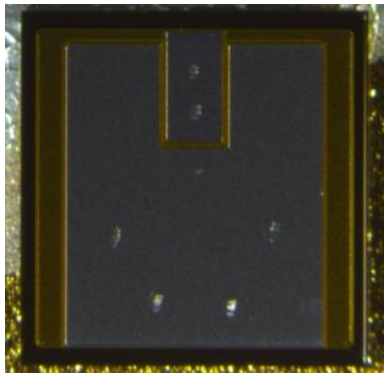


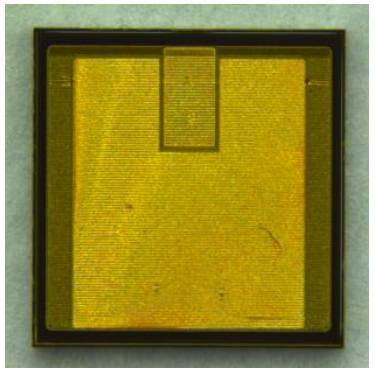


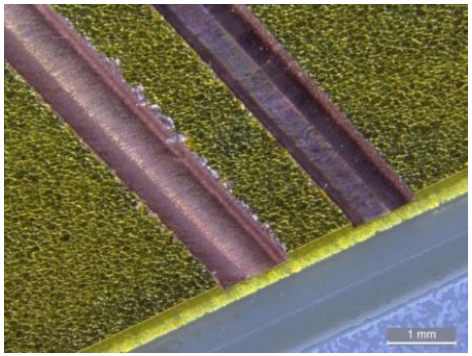


Machining of the DBC Cu-layer

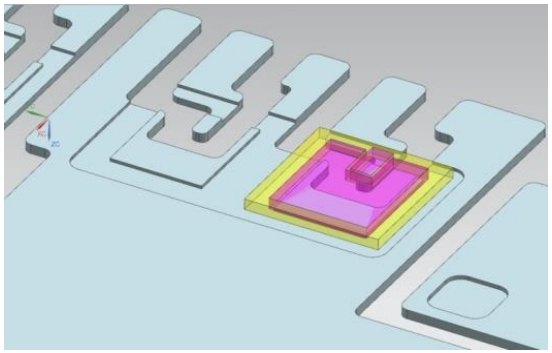
- Electroless Ni/Au plating to prepare surface for sintering process.
- Machining of the Cu layer on the DBC substrates is done to accomplish safe distance to edge frame.



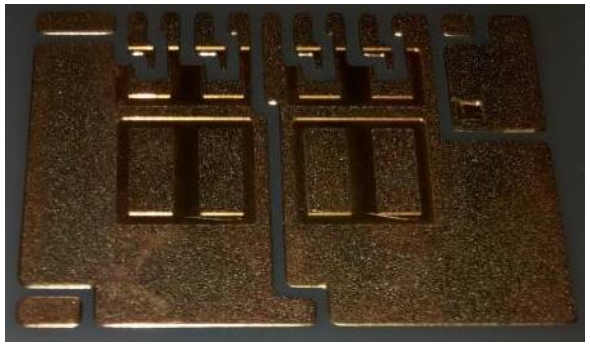




Machining results without (left) and with (right) machining fluid

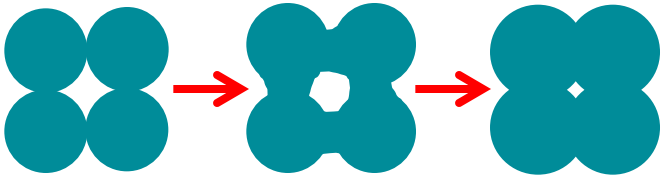


CAD model of the machined substrate

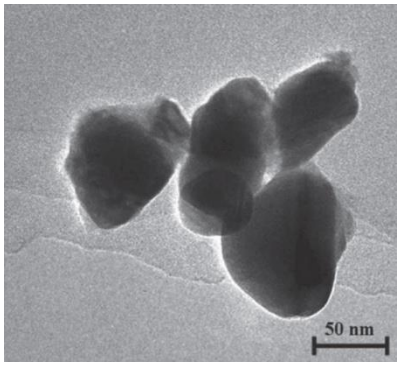


Sintered Die Attach Materials

- Nanoparticles (in organic binder and thinner) sinter together under temperature (and pressure) load.
- Sintering temperature << melting temperature.
- Ag, AgPd, Cu

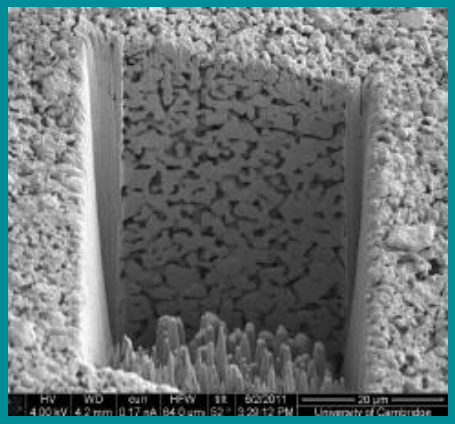


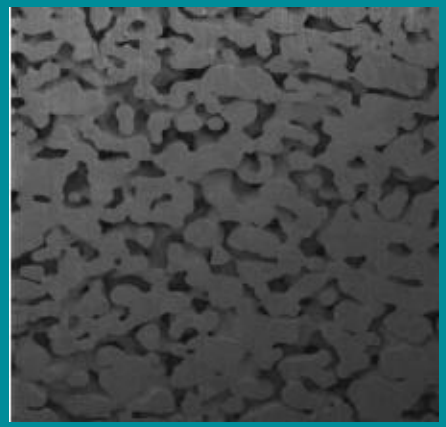
Powder | Structure with open porosity is formed | Closed porosity material



G. Q. Lu, et. al., IEEE Trans. On Device and Materials Reliability, Vol 14, No. 2, June 2014

		Bulk Ag	Nanosilver	SnAg Solder
T_m	°C	961	961	221
Electrial Conductivity	MS/m	68	41	7.8
Thermal Conductivity	W/mK	429	250	70
CTE	µm/mK	19.3	19	28
Tensile Strength	MPa	139	55	30

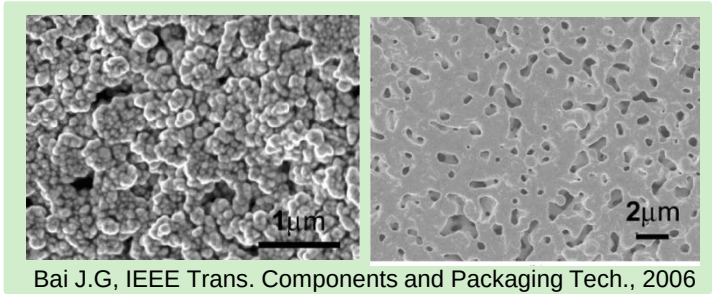




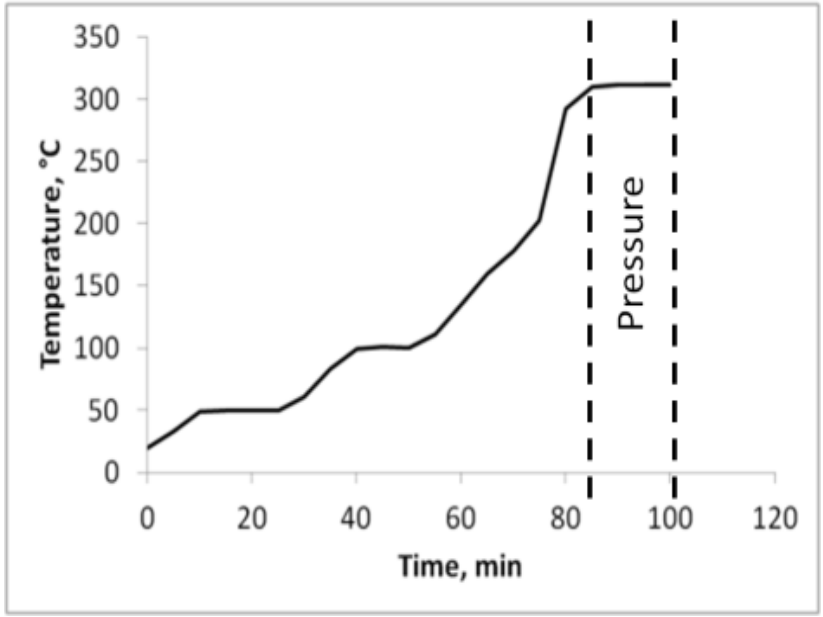
Mills L., ISiCPEAW, May 29-30, 2012, Stockholm, Sweden

Sintering Process

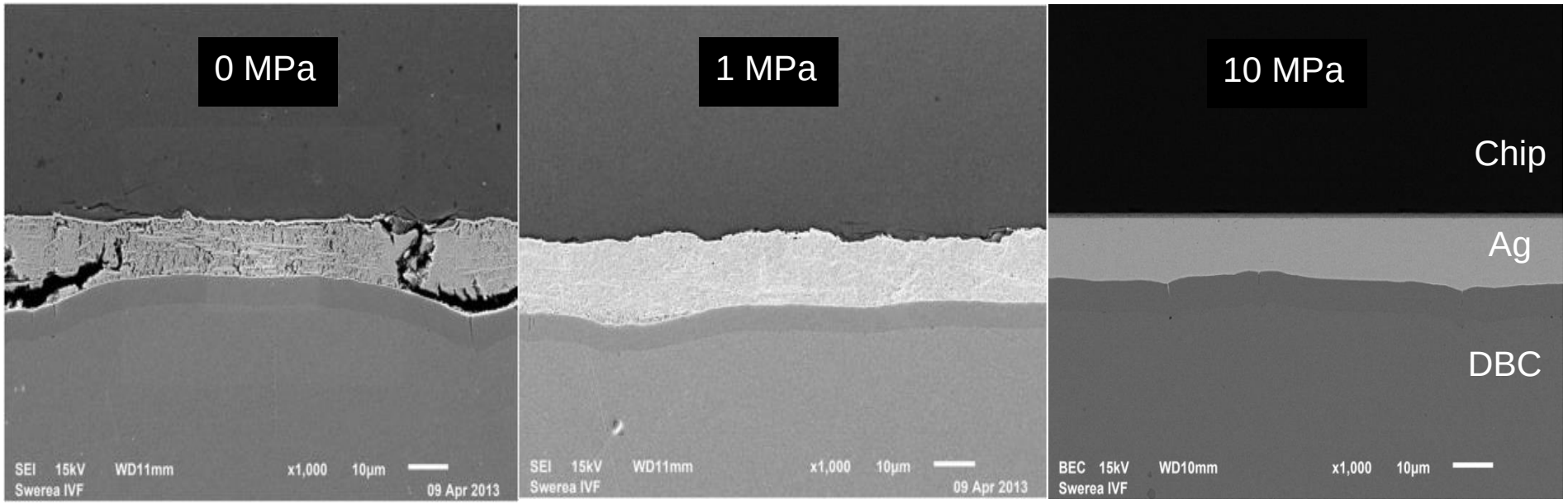
- Screen/stencil-printing
- Drying step
- Placing of device chips
- Sintering process at 200-300 °C
- Pressure applied @ peak temp
- Maintained for 3-5 minutes



Bai J.G, IEEE Trans. Components and Packaging Tech., 2006



Sintering Process



- Temperature, time and pressure control porosity.
- Affects shear strength and reliability of the material

Reliability of Sintered Silver Die Attach

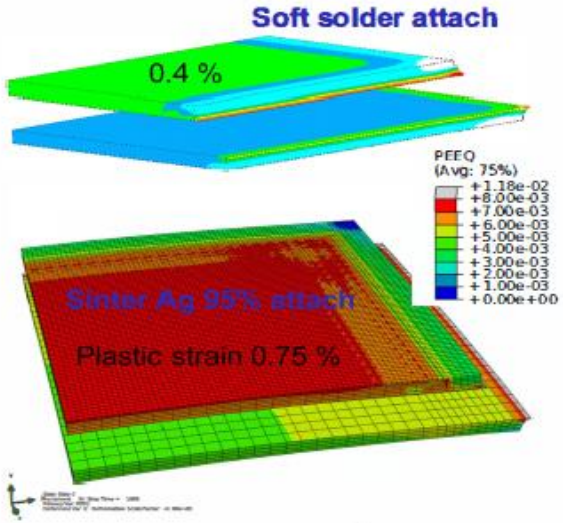
- Melting temperature of silver is much higher than for solder.
- Operational temperature of many applications is comparatively low.
- At normal operating temperatures (- 40 °C - 125 °C):

→ Lead-free solders: $T_{homologous}$ = **0.4** T_m to **0.8** T_m

→ Sintered silver: $T_{homologous}$ = **0.2** T_m to **0.3** T_m

This suggests that fatigue effects during operation should be lower in sintered silver joints compared to solder joints.

- Lack of ductility can also lead to brittle fracture through the die attach layer.
- Higher stiffness, lack of creep and less ductility could generate problems elsewhere in the assembly.
  - Sintered layer does not decouple stresses between the chip and substrate as soldered die attach does.
  - Higher plastic strains in the DBC Cu layer expected from simulations.
  - Failure mechanisms such as DBC fatigue or delamination may become more frequent.

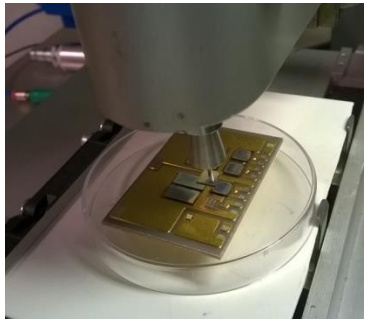
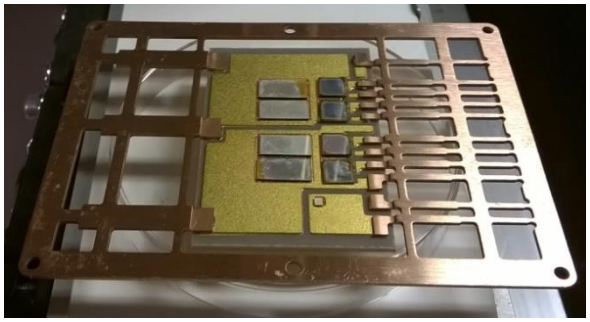
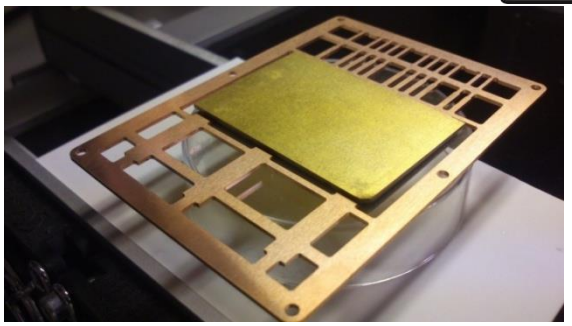


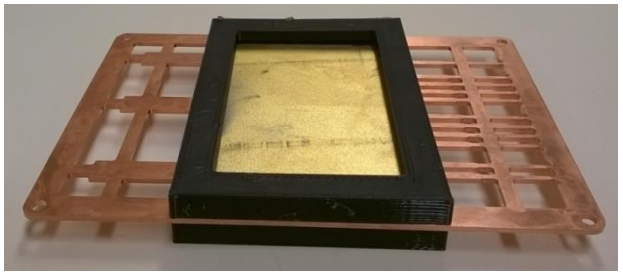
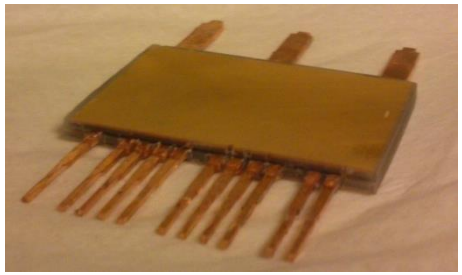
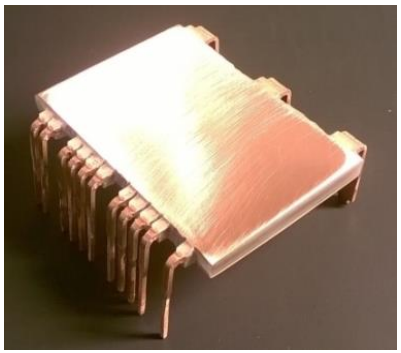
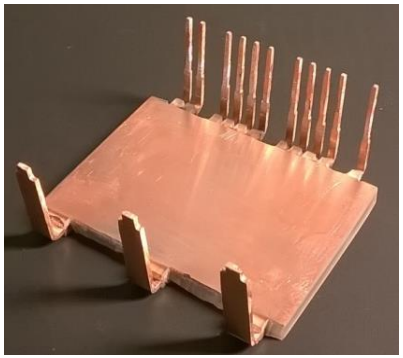
R. Dudek, et. al., EuroSimE 2014.

- 160 million power cycles between +45 and +175 °C extrapolated from a Coffin-Manson model.*
- 5 s, T = 225 °C or pressure of 2 MPa is sufficient to generate bond strength comparable to solder.*
- Good adhesion if process parameters are set correctly.

* M. Knoerr, et al, 12th Electronics Packaging Technology Conference, EPTC 2010; Singapore

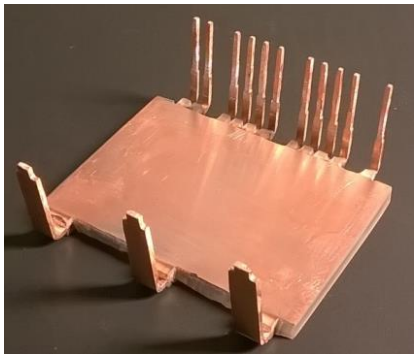
Die Placement, Lead Frame and Molding Steps

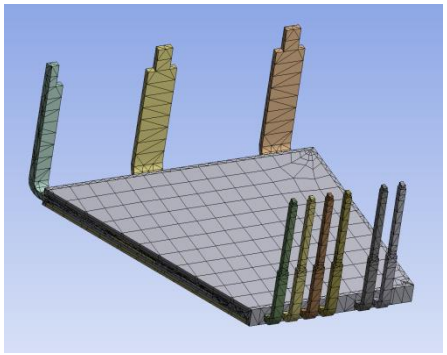




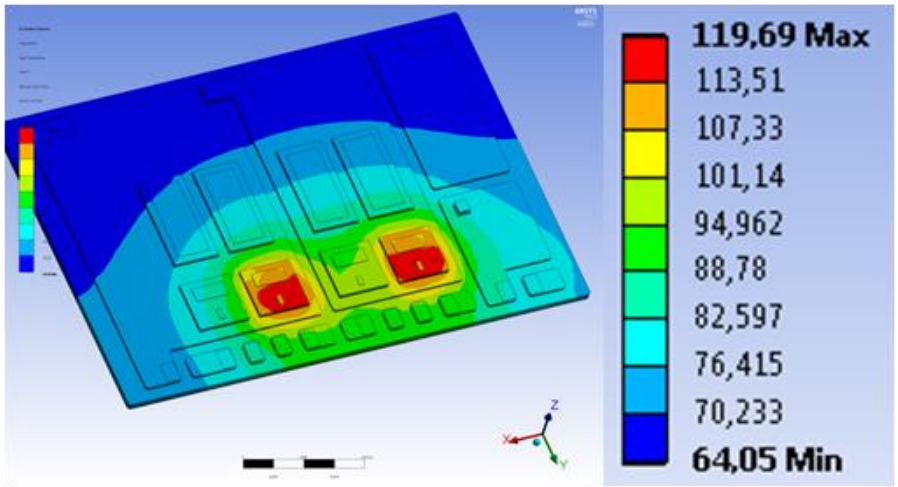





Thermal Models

- Double-sided model with SiC devices sandwiched between AlN DBC substrates molded in epoxy.
- Convection boundary conditions on top and bottom set to 3000 W/(m^{2}K).
- Powering of two transistors (70 W internal heat dissipation each) in three power pulses with a cycle time of 3 s and an ON-time of 1.5 s → Tmax = 119.7 °C.
- Assymetric thermal profile corresponding to top DBC contacting layer (not shown in the figure).



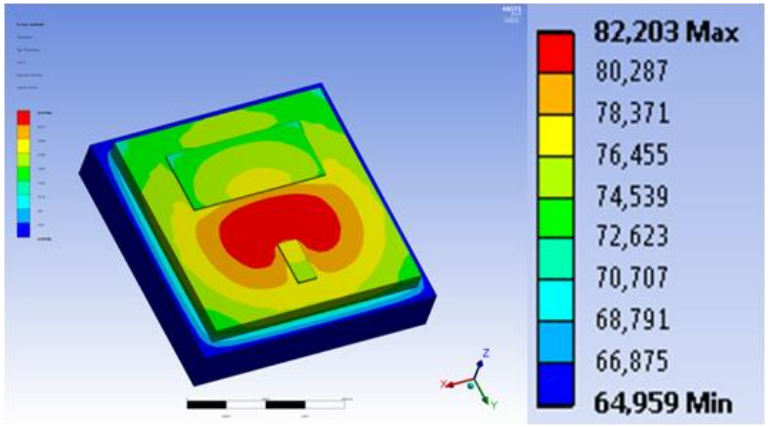




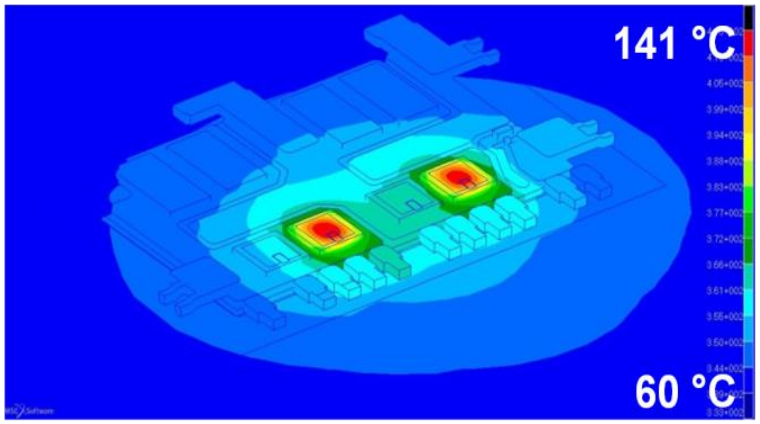
Thermal Models

Two additional thermal simulations:

- A local sub-model containing a slice through all layers over one device chip including 0.5 mm of its surrounding materials in x and y direction.

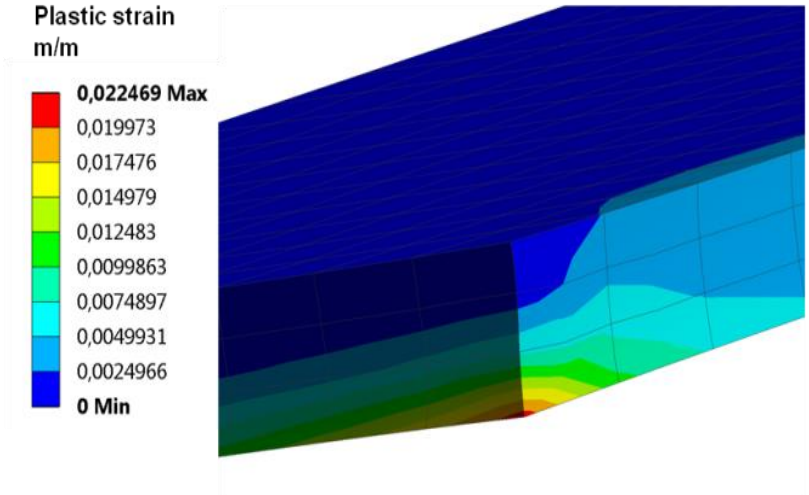


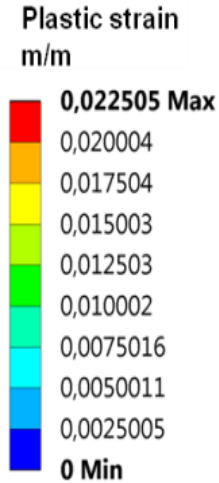
- Single sided cooling version, with SiC devices, lead-free die attach (SAC305) and molding material (bond wires are not included).

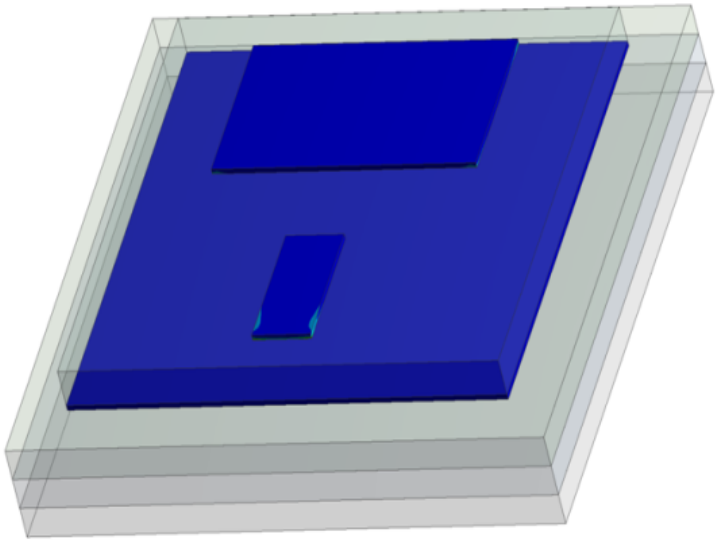


Thermo-Mechanical Results

- 3 power ON cycles of 1.5 s.
- Plastic strain model from Dudek, et. al., EuroSimE 2014.
- Creep model derived from G. Chen et al. 2013.
- No creep strains.
- High plastic strains at corners.
- Plastic strains away from the corners are around to 0.7 %.

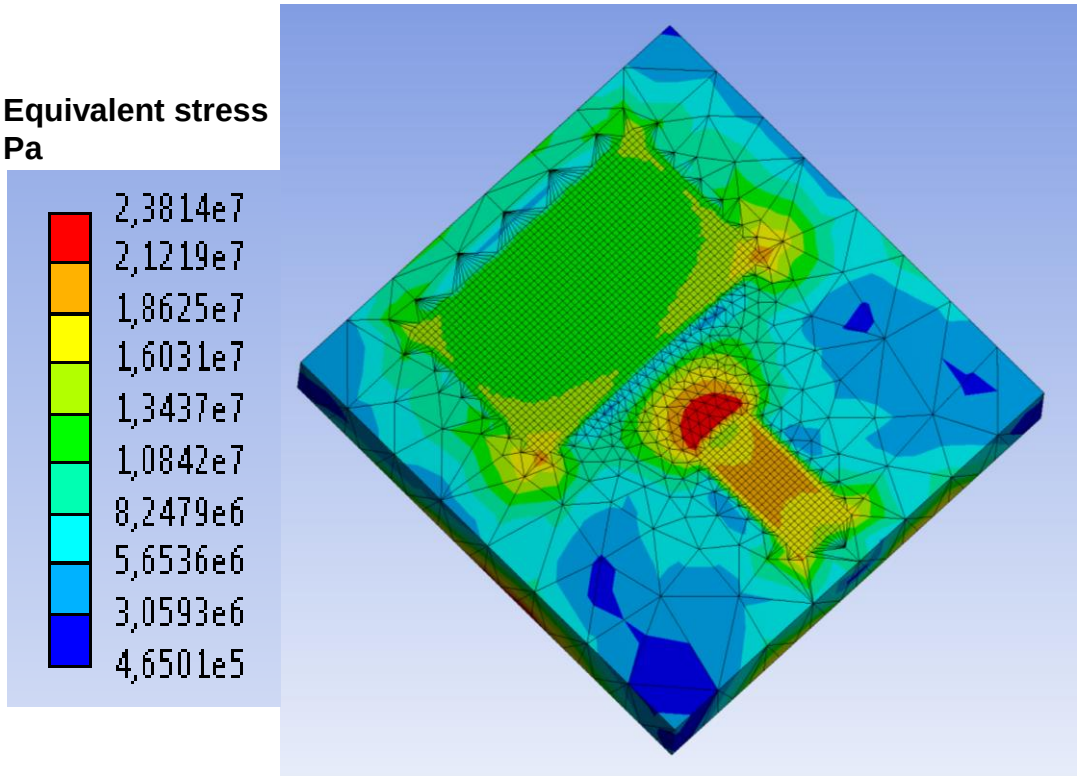






Thermo-Mechanical Results

- Stress on the BJT device chip under top sintered contacts
- Less in the DBC Cu below bottom die attach layer.

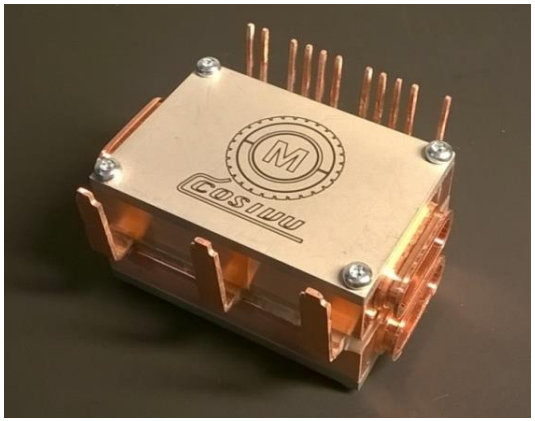


Summary

- A process for fabrication of power modules compatible with double sided cooling has been developed.
- New method to create edge stand-off for high voltage device chips.
- Plating process to prepare for nanosilver process.
- Machining of the substrate Cu layer to allow for edge stand-off distance.
- Device chip design for double sided mounting with larger base pad and Au or Ag metallization on top contacts would be helpful for these types of packages.
- Simulations predict that double sided cooling of power modules can lower the operational temperature by between 15-42 %, which will lead to smaller or fewer devices for a given power requirement specification.

Summary (2)

- Reasons to be carefully optimistic about the reliability of sintered silver die attach.
- Large dependency on process parameters.
- Higher thermal and electrical conductivity, good adhesion, low creep.
- However, lower homologous temperature than solder die attach, which could result in other failures in other parts of the power assembly.
- More long term testing of power assemblies based on sintered die attach material is needed to understand the physics of failure mechanisms.



Thank You for Your Attention!

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